AMENDMENTS

In the Specification:

Please delete the paragraph at page 6, lines 12-19, and replace it with the following:

A1

The following description of the process of the present invention is described in the context of an ONO structure suitable for use in a two-bit EEPROM device, such as the MIRRORBIT™ device. It is to be understood that, while the present invention is discussed herein in that context, that this is merely exemplary and is not intended to limit the scope of the present invention. The ONO structure fabricated by the presently disclosed method is applicable to any semiconductor device in which an ONO structure may be included, and is particularly applicable also to the floating gate FLASH device described above with reference to Fig. 2.

Please delete the paragraph at page 7, lines 3-11, and replace it with the following:

A2

Those skilled in the art will recognize that for proper functioning of a two-bit EEPROM device, the electrical charges 34a, 34b should remain isolated in the regions of the silicon nitride layer 30 to which each is initially introduced. The proper maintenance of the electrical charges 34a, 34b in localized regions of the silicon nitride layer 30 is needed for the proper performance of a two-bit EEPROM device. In particular, the quality of the ONO structure 26 should be such that charge leakage paths are minimized at the interface between the tunnel oxide and top oxide layers 28 and 32, and the silicon nitride layer 30. Additionally, the top oxide layer 32 must be of sufficient density, such that charge trapping sites are minimized within the silicon oxide material.